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Atty. Docket No.: 3359-Z

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re application of
Khader S. Abdel-Hafez et al

Application No. 10/691,966 — Group Art Unit 2858

Filed: October 24, 2003 — Examiner John P. Trimmings

For: METHOD AND APPARATUS FOR TESTING ASYNCHRONOUS SET/RESET FAULTS IN A SCAN-BASED INTEGRATED CIRCUIT

APPEAL BRIEF TRANSMITTAL

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Attached hereto is the BRIEF ON APPEAL for the above-identified application. The fee in the amount of $250.00 is submitted herewith.

Petition is hereby made to the Commissioner of Patents and Trademarks to extend the period for filing this Brief on Appeal for five months, so as to expire February 20, 2007. The fee for this extension in the amount of $1,080.00 is included in the attached check.

Any additional fees necessary to effect the proper and timely filing of this Brief may be charged to Deposit Account No. 26-0090.

Respectfully submitted,

Jim Zegeer

Jim Zegeer, Reg. No. 18,957
Attorney for Appellants

Attachments: Brief on Appeal
Check - $1,330.00

02/21/2007 MBERHE 00000011 10691966

02 FC:2255 1080.00 OP

Suite 108
801 North Pitt Street
Alexandria, VA 22314
Telephone: 703-684-8333

Date: February 20, 2007

In the event this paper is deemed not timely filed, the applicant hereby petitions for an appropriate extension of time. The fee for this extension may be charged to Deposit Account No. 26-0090 along with any other additional fees which may be required with respect to this paper.

Atty. Docket No.: 3359-Z

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For: METHOD AND APPARATUS FOR TESTING ASYNCHRONOUS SET/RESET FAULTS IN A SCAN-BASED INTEGRATED CIRCUIT

BRIEF ON APPEAL

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This is an appeal from the final rejection mailed February 16, 2006 of Claims 83 - 106 of the above-identified application.

(i). The Real Party in Interest

The real party in interest is Syntest Technologies, Inc.

(ii). Related Appeals and Interferences

There are no related appeals or interferences.

(iii). Status of the Claims

Claims 83 - 106 are on appeal. All other claims, namely, claims 1 - 82 have been cancelled.

(iv). Status of the Amendments

There was no amendment filed after final action dated February 26, 2006.

(v). Summary of Claimed Subject Matter

The invention generally relates to the field of logic design and test using design for test techniques for testing asynchronous set/reset faults in integrated circuits using scan test techniques.

Each manufactured integrated circuit must be tested in order to verify structural and functional correctness. With the ever-increasing scale and complexity of integrated circuits, the goal of achieving high test quality at a reasonable cost is becoming extremely difficult. Therefore, improving the inherent testability on an integrated circuit is imperative in order to realize this goal (the specification at page 2, lines 8 - 12).

In a scan-based integrated circuit, the original memory elements, comprising flip-flops and/or latches, are replaced with scan-equivalent storage elements, called scan cells. These scan cells are allowed to select one of two possible data sources depending on the state of a selected scan enable (SE) signal. When SE is set to logic value 0, the normal data input port is selected. When SE is set to logic value 1, the scan input port is selected. The scan input ports and scan output ports of all scan cells are stitched together in a way so that the scan cells are reconfigured as one or more shift registers called scan chains. These scan

chains are either accessed internally during self-test or through external scan input ports and scan output ports during scan-test (the paragraph bridging pages 2 and 3 of the specification).

Three operations are used to test a scan-based integrated circuit. These operations are shift-in, capture and shift-out (specification, page 3, lines 9 and 10).

The specification at pages 3 - 4 describe further background features of the invention. Pages 5, 6 and the top of page 7 provide background on prior art solutions set out in Figs. 2B, 2C, 2D and 2E of the drawings. The problem with these different solutions is set out at pages 7 and 8 of the specification.

Fig. 3A shows a block diagram 300 of two set/reset controllers in a design without any ripple structure, in accordance with the present invention. A set/reset controller 303, is controlled by a local scan enable signal SE1 315 and a local set/reset enable signal SR_EN1 316, consists of a capture controller 305 and a shift controller 306. The set/reset controller 304, controlled by a local scan enable signal SE2 317 and a local set/reset enable signal SR_EN2 318, consists of a capture controller 307 and a shift controller 308. The local scan enable signals SE1 315 and SE2 317 are driven by a global scan enable signal global_SE 312. The local set/reset enable signals SR_EN1 316 and SR_EN2 318 are driven by a global set/reset enable signal global_SR_EN 311. Note that the global scan enable signal global_Se 312 and the global set/reset enable signal global_SR_EN 311 are either generated in the scan-

based integrated circuit under test or provided as an input signal to the scan-based integrated circuit. In addition, it is assumed that there is no path from the Q output 326 of the scan cell SC2 310 to the set/reset circuitry 301 and that there is no path from the Q output 325 of the scan cell SC1 309 to the set/reset circuitry 302. That is, there is no ripple structure existing between the two scan cells SC1 309 and SC2 310. (Specification pages 29-30.)

A set/reset controller can avoid race conditions and glitches that may arise in the prior art, while preserving its capability of detecting asynchronous set/reset faults in a scan-based integrated circuit. For example, the set/reset controller 303 consists of the capture controller 305 and the shift controller 306. The set/reset controller 303 provides a new asynchronous set/reset signal 319, controlled by two enable signals, namely, the scan enable SE1 315 and the set/reset enable SR_EN1 316. The shift controller 306 is used to guarantee that the new asynchronous set/reset signal 319 remains disabled during the shift operation in order to avoid destroying any data that are being shifted into the scan cell 309. The capture controller 305, together with the shift controller 306, is used to realize a two-stage control on the new asynchronous set/reset signal 319 during the capture operation to guarantee that faults present in the original asynchronous set/reset circuitry 301 are detected without any race condition or glitch. (Specification, page 30.)

At the first stage of the capture operation, the SR_EN1 signal 316 is set to logic value 0, and capture clocks are applied to capture the test response into all scan cells through their data ports. At this stage, the new asynchronous set/reset signal 319 is disabled, ensuring that no race conditions and glitches arise. At the second stage of the capture operation, the SR_EN1 signal 316 is set to logic value 1 while disabling all capture clocks to allow the faults present in the original asynchronous set/reset circuitry 301 to be propagated via 319 to the scan cell 309. As a result, the faults present in the original asynchronous set/reset circuitry 301 can be detected. (Specification, page 31.)

FIG. 3B shows a block diagram 330 of three set/reset controllers in a design with a two-stage ripple structure, in accordance with the present invention and is described more fully at pages 31-33.

FIG. 4A shows a timing diagram 400a for testing the design without any ripple structure shown in FIG. 3A, in accordance with the present invention, where both data faults and set/reset faults are detected during the same capture operation with non-overlapping single-capture clocks. In one test pattern, 401a, 402a and 403a designate the shift-in operation, capture operation and shift-out operation, respectively. During the first cycle in the capture operation 402a, two single pulses are applied to the capture clocks CK1 322 and CK2 324 in a non-overlapping manner as shown at 405a and 406a to detect data faults while the global set/reset enable

global_SR_EN 311 is set to logic value 0. This non-overlapping capture clock scheme is used to avoid the impact of clock skews between two clock domains. Then, during the second cycle in the same capture operation 402a, the global set/reset enable global_SR_EN 311 is set to logic value 1 as shown at 404a while the capture clocks CK1 322 and CK2 324 are inactive; as a result, set/reset faults are detected. (Specification, page 24.)

FIG. 4B shows a timing diagram 410a for testing the design without any ripple structure shown in FIG. 3A, in accordance with the present invention, where both data faults and set/reset faults are detected during the same capture operation with overlapping single-capture clocks and is described more fully at pages 34-35.

FIG. 4C shows a timing diagram 420a for testing the design without any ripple structure shown in FIG. 3A, in accordance with the present invention, where both data faults and set/reset faults are detected during the same capture operation with non-overlapping at-speed double-capture clocks and is described more fully at pages 35-36 of the specification.

FIG. 4D shows another a timing diagram 430a for testing the design without any ripple structure shown in FIG. 3A, in accordance with the present invention, where both data faults and set/reset faults are detected during the same capture operation with overlapping at-speed double-capture clocks and is described more fully at page 36 of the specification.

FIG. 4E shows another timing diagram 440a for testing the design without any ripple structure shown in FIG. 3A, in accordance with the present invention, where data faults and set/reset faults are detected during two capture operations with non-overlapping single-capture clocks and is described more fully at page 37 of the specification.

FIG. 4F shows another timing diagram 450a for testing the design without any ripple structure shown in FIG. 3A, in accordance with the present invention, where data faults and set/reset faults are detected during two capture operations with non-overlapping at-speed double-capture clocks and is described more fully at pages 37-38 of the specification.

FIG. 4G shows a timing diagram 400b for testing the design with a two-stage ripple structure shown in FIG. 3B, in accordance with the present invention, where both data faults and set/reset faults are detected during the same capture operation with non-overlapping single-capture clocks and is described more fully at page 38 of the specification.

FIG. 4H shows a timing diagram 410b for testing the design with a two-stage ripple structure shown in FIG. 3B, in accordance with the present invention, where both data faults and set/reset faults are detected during the same capture operation with non-overlapping at-speed double-capture clocks and is described more fully at page 39 of the specification.

FIG. 4I shows a timing diagram 430b for testing the design with a two-stage ripple structure shown in FIG. 3B, in accordance with the present invention, where data faults and set/reset faults are detected during two capture operations with non-overlapping single-capture clocks and is described more fully at page 40 of the specification.

Finally, FIG. 4J shows a timing diagram 450b for testing the design with a two-stage ripple structure shown in FIG. 3B, in accordance with the present invention, where data faults and set/reset faults are detected during two capture operations with non-overlapping at-speed double-capture clocks and is described more fully in the paragraph bridging pages 40 and 41.

(vi). Grounds of Rejection to be Reviewed on Appeal

Ground 1.

The denial of domestic priority.

Ground 2.

The rejection of claim 83 -106 under 35 U.S.C. 103(a) as being unpatentable over Ahanin et al (US 5,166,604) (hereinafter Ahanin), in view of appellants' admitted prior art (herein AAPA) in view of Wang et al (US 2002/0120896) (hereinafter Wang) and further in view of "ORCA® Series 4 FPGAs" by Lattice Semiconductor (hereinafter Lattice).

(vii). Argument

As to Ground No. 1:

The Examiner's denial of domestic priority on the ground that the provisional application Serial No. 60/422,117 does not have a reference to "global scan enable and global set/reset enable signals" is in error. In this regard, reference is made to appellants' provisional specification (PS), page 3, first full paragraph reading:

> The present invention uses a scan enable (SE) and and/or gate to disable the asynchronous set/reset signals of all scan cells. A new set/reset enable (SR_EN) signal is introduced to propagate the faults of asynchronous set/reset signals in a dedicated capture cycle. In this dedicated capture cycle, the test clocks are disabled so that the race conditions that exist on prior-art #3 are eliminated. The present invention repairs the asynchronous set/reset violations either at the register transfer level (RTL) or the gate-level circuit.

Also, appellants' SUMMARY of the invention at PS page 4 reads as follows:

Three additional input signals, a scan enable signal SE a test enable signal TE and a set/reset enable (SR_EN) signal can be added to the RTL codes for this purpose. The three enable signals, SE, TE, and SR_EN will be used to control the operation of added scan logic so that the circuit can function correctly during scan and normal operations. The following table summarizes the circuit operation mode under different SE, TE, and SR_EN values. The test clocks are disabled during the capture set/reset mode.

TE	SE	SR_EN	Mode
0	0	1	normal
1	1	x	shift
1	0	0	capture data
1	0	1	capture set/reset

While the word "global" is not used, taken with the drawings, these all imply that the scan-enable SE signals and the set/reset enable SR_EN signals are global in nature.

As to Ground No. 2,

The rejection of claims 83 - 106 under 35 U.S.C. 103(a) as being unpatentable over (1) Ahanin in view of (2) appellants' admitted prior art in view of (3) Wang further in view of (4) Lattice is clearly in error and is based on hindsight reconstruction of the art herein.

The urge and impetus to make the Ahanin AAPA, Wang and Lattice combination is not suggested or taught in any of the references and

is dictated by hindsight rather than patentable obviousness. Ahanin uses "one" PRESET/CLEAR DISABLE signal to test each asynchronous NPRESET/NCLEAR port (see Fig. 2 in Ahanin). Since a real design can use many PRESET/CLEAR DISABLE signals, Ahanin further disclosed an example test circuit in Fig. 3 to generate these TEST CONTROL SIGNALS. The example test circuit is not perfect because it creates "new" asynchronous set/reset violations (see Q to CLRN in Fig. 3), uses an additional TEST CONTROL pin as the test CLOCK, and introduced a number of non-scan D flip-flops to save the TEST CONTROL SIGNALS. Ahanin does <u>not</u> point out how to test the newly created set/reset logic (Q to CLRN) and non-scan flip-flops, rendering Fig. 3 not quite practical in real applications.

There is another solution to use a shift register to generate these internal TEST CONTROL SIGNALS, but shifting could potentially destroy the contents of each flip-flop. Ahanin does <u>not</u> teach how to prevent the data from being corrupted due to shifting, though schemes are available using an additional input signal or internal register.

These problems are solved by the present application discovery that using one control signal for testing each asynchronous set/reset port is not good enough; the test circuit hardware is large and the test circuit may not be tested.

In regard to the Examiner's reference to AAPA (Fig. 2D prior art disclosure in the present application):

This prior art using one global SE to test set/reset is simple because it allows to disable all set-reset during scan shift. The problem is this SE is only one pin, so if there are ripple set/reset circuitries (or loops), a race condition can occur. This will cause significant fault coverage drop and is no longer a practical solution.

Therefore, the present invention uses one global scan enable (global_SE) in addition to using only "one" global set/reset enable (global_SR_EN) signal. See Fig. 3A and Fig. 3B in the present application. See independent claims 83 and 96. The global_SE signal can globally disable all set/reset ports so that during shifting using the above shift register solution, all flip-flop contents are preserved. Since scan enable is a must for scan-based designs, we need not to use any additional pin for global_SE. In addition, we can shift in all global_SR_EN signals through TDI using the IEEE 1149.1 Boundary-scan Standard when required. Therefore, the present invention virtually does not need any additional input signal pin when each global_SR_EN signal is qualified by the global scan enable (global_SE) signal. And the test circuit hardware is small.

The only portion of Lattice referred to by the Examiner is the third paragraph on page 32 reading as follows:

> Each PIC contains up to four programmable I/O (PIO) pads and are interfaced through a common interface block (CIB) to the FPGA array. The PIC is split into two pairs of I/O pads with each pair having independent clocks, clock enables, local set/reset, and global set/reset enable/disable.

Clearly, the using appellants' teaching as a guide, Examiner has merely reached into the reference and extracted the global set/reset (which is discussed further in the left column of page 39). It is a different global set/reset and operates differently than appellants' global set/reset. The Examiner has extracted words without their functional equivalent and used them in the combination to reject the claims. Clearly, this is in error.

CONCLUSION

In conclusion, the Examiner has erred in rejecting claims 83 - 106 and should be reversed.

Respectfully submitted,

Jim Zegeer

Jim Zegeer, Reg. No. 18,957
Attorney for Appellants

Attachments: CLAIMS APPENDIX
EVIDENCE APPENDIX

Suite 108
801 North Pitt Street
Alexandria, VA 22314
Telephone: 703-684-8333

Date: February 20, 2007

In the event this paper is deemed not timely filed, the applicant hereby petitions for an appropriate extension of time. The fee for this extension may be charged to Deposit Account No. 26-0090 along with any other additional fees which may be required with respect to this paper.

(viii) CLAIMS APPENDIX

83. A method for testing faults propagated to the data ports and asynchronous set/reset ports of selected scan cells in a scan-based integrated circuit in a selected scan-test mode or selected self-test mode using a global scan enable (global_SE) signal and one or more global set/reset enable (global_SR_EN) signals, the scan-based integrated circuit containing one or more set/reset circuitries each controlled by a set/reset controller, and one or more scan chains, each scan chain comprising multiple scan cells coupled in series, each scan cell having one or more clocks and each set/reset controller connected to said global scan enable (global_SE) signal and one said global set/reset enable (global_SR_EN) signal; said method comprising:

(a) shifting in a stimulus to all said scan cells in said scan-based integrated circuit by enabling said global scan enable (global_SE) signal through all said set/reset controllers to disable all said set/reset circuitries during a shift-in operation;

(b) capturing a test response of all said scan cells for testing said faults propagated to said data ports and said asynchronous set/reset ports of all said selected scan cells by enabling or disabling selected global set/reset enable (global_SR_EN) signals while disabling said global scan enable (global_SE) signal during a capture operation;

(c) shifting out said test response for comparison or compaction while shifting in a new stimulus to all said scan cells during a shift-out operation.

84. The method of claim 83, wherein said shifting in a stimulus to all said scan cells further comprises selectively shifting in a predetermined stimulus from an ATE (automatic test equipment) in said selected scan-test mode or shifting in a pseudo-random stimulus automatically generated in said scan-based integrated

circuit using a pseudo-random pattern generator (PRPG) in said selected self-test mode during said shift-in operation.

85. The method of claim 83, wherein said global scan enable (global_SE) signal is further used to enable shifting a scan data from a first scan cell to a second scan cell during said shift-in and said shift-out operation.

86. The method of claim 83, wherein said capturing a test response of all said scan cells further comprises disabling all said clocks controlling all said scan cells, while enabling all said selected global set/reset enable (global_SR_EN) signals, for testing said faults propagated to said asynchronous set/reset ports of said selected scan cells during said capture operation.

87. The method of claim 86, wherein said enabling all said selected global set/reset enable (global_SR_EN) signals further comprises selectively enabling two or more said selected global set/reset enable (global_SR_EN) signals simultaneously or in an ordered sequence during said capture operation.

88. The method of claim 83, wherein said capturing a test response of all said scan cells further comprises enabling all said clocks controlling all said scan cells, while disabling all said selected global set/reset enable (global_SR_EN) signals, for testing said faults propagated to said data ports of all said selected scan cells during said capture operation.

89. The method of claim 88, wherein said enabling all said clocks controlling all said scan cells further comprises selectively enabling two or more said clocks controlling two or more said scan cells simultaneously or in an ordered sequence during said capture operation.

90. The method of claim 83, wherein said shifting out said test response for comparison or compaction further comprises selectively shifting out said test response to said ATE for comparison in said selected scan-test mode or shifting out said test response for compaction using a compactor, including a multiple-input signature register (MISR), in said selected self-test mode during said shift-out operation.

91. The method of claim 83, wherein said set/reset controller further comprises providing a shift controller and a capture controller in response to said global scan enable (global_SE) signal and a said global set/reset enable (global_SR_EN) signal, wherein said shift controller is adapted to disable said asynchronous set/reset ports of one or more said selected scan cells during said shift-in or said shift-out operation, and wherein said capture controller is adapted to enable or disable propagation of said faults present in one said set/reset circuitry to said asynchronous set/reset ports of one or more said selected scan cells during said capture operation.

92. The method of claim 83, wherein said global scan enable (global_SE) signal is selectively generated in said scan-based integrated circuit or an input signal to said scan-based integrated circuit.

93. The method of claim 83, wherein said global set/reset enable (global_SR_EN) signal is selectively generated in said scan-based integrated circuit or an input signal to said scan-based integrated circuit.

94. The method of claim 83, wherein said scan cell is selectively a multiplexed-type D flip-flop, a two-port D flip-flop, or a LSSD (level-sensitive scan design) SRL (shift register latch).

95. The method of claim 83, wherein said set/reset controller is used to repair one or more asynchronous set/reset violations, comprising sequentially-gated set/reset violations, combinationally-gated set/reset violations, generated set/reset violations, and destructive set/reset violations, in a selected set/reset circuitry in said scan-based integrated circuit.

96. A set/reset controller having a global scan enable (global_SE) signal and a global set/reset enable (global_SR_EN) signal for testing faults propagated to the data ports and asynchronous set/reset ports of selected scan cells in a scan-based integrated circuit, the scan-based integrated circuit containing one or more set/reset circuitries and one or more scan chains, each scan chain comprising multiple scan cells coupled in series, each scan cell having one or more clocks; said set/reset controller comprising:

(a) a shift controller, inserted between a selected set/reset circuitry and said asynchronous set/reset ports of all said selected scan cells, for disabling said asynchronous set/reset ports of all said selected scan cells, when said global scan enable (global_SE) signal is enabled, during a shift-in or a shift-out operation; and

(b) a capture controller, inserted between said selected set/reset circuitry and said asynchronous set/reset ports of all said selected scan cells, for enabling or disabling propagation of said faults present in said selected set/reset circuitry to said asynchronous set/reset ports of all said selected scan cells, in response to said global set/reset enable (global_SR_EN) signal when said global scan enable (global_SE) signal is disabled, during a capture operation.

97. The set/reset controller of claim 96, wherein said shift controller is selectively embedded in said selected set/reset circuitry or in all said selected scan cells, and wherein said global scan enable (global_SE) signal, said global set/reset enable

(global_SR_EN) signal, or said global scan enable (global_SE) signal and said global set/reset enable (global_SR_EN) signal can be selectively used to disable all said asynchronous set/reset ports of all said selected scan cells during said shift-in or said shift-out operation.

98. The set/reset controller of claim 96, wherein said global scan enable (global_SE) signal is further used to enable shifting a scan data from a first scan cell to a second scan cell during said shift-in and said shift-out operation.

99. The set/reset controller of claim 96, wherein said capture controller further comprises disabling all said clocks controlling all said scan cells, while enabling said global set/reset enable (global_SR_EN) signal, for testing said faults propagated to said asynchronous set/reset ports of all said selected scan cells during said capture operation.

100. The set/reset controller of claim 96, wherein said capture controller further comprises enabling all said clocks controlling all said scan cells, while disabling said global set/reset enable (global_SR_EN) signal, for testing said faults propagated to said data ports of said selected scan cells during said capture operation.

101. The set/reset controller of claim 100, wherein said enabling all said clocks controlling all said scan cells further comprises selectively enabling two or more said clocks controlling two or more said scan cells simultaneously or in an ordered sequence during said capture operation.

102. The set/reset controller of claim 96, wherein said capture controller is selectively embedded in said selected set/reset circuitry or in all said selected scan cells.

103. The set/reset controller of claim 96, wherein said global scan enable (global_SE) signal is selectively generated in said scan-based integrated circuit or an input signal to said scan-based integrated circuit.

104. The set/reset controller of claim 96, wherein said global set/reset enable (global_SR_EN) signal is selectively generated in said scan-based integrated circuit or an input signal to said scan-based integrated circuit.

105. The set/reset controller of claim 96, wherein said scan cell is selectively a multiplexed-type D flip-flop, a two-port D flip-flop, or a LSSD (level-sensitive scan design) SRL (shift register latch).

106. The set/reset controller of claim 96, wherein said shift controller and capture controller are used to repair one or more asynchronous set/reset violations, comprising sequentially-gated set/reset violations, combinationally-gated set/reset violations, generated set/reset violations, and destructive set/reset violations, in said selected set/reset circuitry in said scan-based integrated circuit.

(ix). EVIDENCE APPENDIX

None.

(x). RELATED PROCEEDINGS APPENDIX

There are no proceedings as mentioned in section (i) above, and accordingly no decisions rendered.